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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

EIJI SAKAGAMI :EXAMINER: H. WEISS

SERIAL NO.: 09/955,076 :

FILED: SEPTEMBER 19, 2001 :GROUP ART UNIT: 2814

FOR: NONVOLATILE SEMICONDUCTOR MEMORY
AND METHOD OF FABRICATING THE SAME

REQUEST FOR RECONSIDERATION

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

This communication is responsive to the final Official Action dated November 8, 2002.

Claims 1-6 are presently active.

In the outstanding Office Action, Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al (U.S. Pat. No. 6,255,166) and Inoue (U.S. Pat. No. 5,559.048). Claims 2, 3, and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue in view of Resinger (U.S. Pat. No. 6,137,718). Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue and Resinger in view of Agarwal et al (U.S. Pat. No. 6,201,276). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue in view of Fang (U.S. Pat. No. 6,023,085).

Briefly, Claim 1 defines a semiconductor memory including first and second transistors isolated by a trench and including a charge storage layer in a first gate insulator of

the first transistor. The charge storage layer is restricted from an element isolation region and exists only below a first gate electrode of the first transistor in an element region.

The final Office Action asserts that Claim 1 is obvious over Ogura et al in view of Inoue. However, M.P.E.P. §2143.03 requires that, to establish a case of *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. Neither Ogura et al nor Inoue disclose or suggest a charge storage layer existing only below a first gate electrode in an element region and restricted from an element isolation region, as defined in Claim 1.

In response to the previously filed arguments, the final Office Action asserts that Fig. 1 of Ogura et al. specifically shows charge storage layer 132b existing only below a first gate electrode G2[1]. However, Ogura et al do not show a cross sectional view perpendicular to the cross sectional view shown in Fig. 1, and do not disclose a cross sectional view showing an element region and an element isolation region.

Applicant submits that one of ordinary skill in the art would assume that Ogura et al uses a conventional method such as for example local oxidation of silicon (LOCOS) isolation to form the disclosed non-volatile memory cell. In conventional LOCOS isolation, a gate insulator (such as for example insulator 132 in Ogura et al) including a charge storage layer (such as for example layer 132b in Ogura et al) would be patterned after formation of the element isolation region. Therefore, a photomask used in the step of forming the element isolation region differs from a photomask used in the step of forming the charge storage layer 132b, so that there exists mask misalignment between these two photomasks. Conventionally, a photomask used in the step for element isolation is patterned so as to have

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[1]Office Action, page 5, lines 9-10.

an opening portion over the element isolation region. The opening portion is required to be smaller than a width of the element isolation region to accommodate mask alignment tolerance. This is because, if the opening portion of the photomask used for element isolation were to be larger than the width of the element isolation region and extend over a channel region, a gate insulator region would be exposed at the opening portion. As a result, a deposited gate (such as for example gate 142 in Ogura et al.) would contact a surface of the substrate 10 directly, and a short circuit would occur between for example gate 142 and substrate 10 in Ogura et al.

For these reasons, the opening portion of the photomask in conventional processing used for element isolation is smaller than the width of the element isolation region to prevent accidental shorting of the gate electrode to the substrate. Hence, one of ordinary skill in the art, without disclosure to the contrary, would assume that the gate insulator 132 in Ogura et al including charge storage layer 132b included as part of the gate insulator 132 extends over the element isolation region to avoid shorting of the gate electrode to the substrate.

Accordingly, the feature of a charge storage layer existing only below a first gate electrode, as defined in Claim 1, is not disclosed or suggested in Ogura et al.

Further, Applicants submits that the deficiencies of Ogura et al are not overcome by the teachings of Inoue.

Inoue shows in both Fig. 8A and 9G a double layered floating gate EPROM having a first floating gate 103, a second floating gate 106, and a control gate 110. Electrons are injected into the first floating gate 103. As discussed in our previously filed remarks, the second floating gate 106 in Inoue is formed on the first floating gate 103 so that the electric charge injected into the first floating gate 103 diffuses from the first floating gate 103 to the second floating gate 106. Because these two gates 103 and 106 are directly contacted and

made of a conductive material, the potentials on these two gates 103 and 106 become uniform. As a result, the electric charge injected into the first floating gate 103 diffuses into the portions of the second floating gate 106 which extend above source/drain regions 104. Thus, the amount of the electric charge remaining in the first floating gate 103 over the channel region reduces due to the charge diffusion into the second floating gate 106. Thus, Inoue does not disclose a charge storage layer existing only below the first gate electrode (i.e., existing only below first gate electrode 103b), as charge injected into the disclosed first gate electrode of Inoue diffuses to the disclosed second gate electrode and exists beyond a region below the first gate electrode.

Accordingly, the feature of a charge storage layer existing only below the first gate electrode, as defined in Claim 1, is not disclosed or suggested in Inoue.

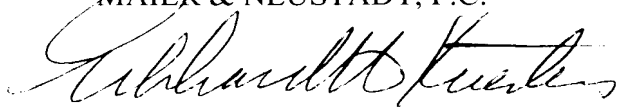
Thus, within the above-noted features set forth in Claim 1 not being disclosed or suggested in either Ogura et al. or Inoue, a case of *prima facie* obviousness has not been established. Hence, Claim 1 is not made obvious in view of the applied prior art.

Thus, it is respectfully submitted that Claim 1 and Claims 2-6 which depend from Claim 1 patentably define over the applied prior art.

Consequently, in view of the above discussions, the outstanding grounds for rejection are believed to have been overcome. This application is believed to be in a condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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